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| First Named Inventor | Leonard Forbes |
| Serial No. | 10/714,753 |
| Filing Date | November 17, 2003 |
| Group Art Unit | 2818 |
| Examiner Name | Unknown |
| Confirmation No. | 3377 |
| Attorney Docket No. | 400.260US01 |

**GENERAL
TRANSMITTAL
FORM UNDER 37 CFR 1.8
(LARGE ENTITY)**

Title: NROM FLASH MEMORY DEVICES ON ULTRATHIN SILICON

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Enclosures

The following documents are enclosed:

- Information Disclosure Statement (1 pgs.); Form 1449 (7 pgs.); 58 copies of cited references; U.S. reference(s) not included pursuant to 37 C.F.R. 1.98 (c)(2)(i);
- An itemized return-receipt postcard

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Submitted By

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| Name | Kenneth W. Bolvin | Reg. No. | 34,125 | Telephone | (612) 312-2211 |
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Certificate of Mailing

I certify that this correspondence and the identified documents listed on this transmittal are being deposited with the United States Postal Service with sufficient postage as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 on May 24, 2004.

| | | | |
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| Name | Rhonda L. Foley | Signature | |
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(LARGE ENTITY TRANSMITTAL UNDER 37 CFR § 1.8)



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In compliance with 37 C.F.R. §§ 1.56 and 1.97, *et seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified Application. Pursuant to 37 C.F.R. 1.98 (a)(2)(i), as this application was filed after June 30, 2003, Applicant has not included copies of U.S. Patents or U.S. Patent Applications. Applicant respectfully requests that this Information Disclosure Statement be entered and the references listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to MPEP §609, Applicant further requests that the Examiner initial next to each reference on the Form 1449 to indicate that the listed references have been considered. Applicant further requests that a copy of the initialed Form 1449 be returned with the next official communication.

As an Office Action has not yet issued in this application, Applicant believes that no fees are due. However, the Commissioner for Patents is hereby authorized to charge any additional fees to Deposit Account No. 501373. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211.

Respectfully submitted,

Date: 5/24/04

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INFORMATION DISCLOSURE STATEMENT

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|---|-------------------|---|
| First Named Inventor | Leonard Forbes | INFORMATION DISCLOSURE STATEMENT FORM PTO-1449 |
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| U.S. Patent References | | | | |
|-------------------------------|-----------------|------------------------|--------------|-------------|
| Examiner Initials | Document No. | Issue/Publication Date | Name | Filing Date |
| | 2001/0001075 A1 | 05/10/2001 | Ngo | 12/20/2000 |
| | 2001/0004332 A1 | 06/21/2001 | Eitan | 02/07/2001 |
| | 2001/0011755 A1 | 08/09/2001 | Tasaka | 09/16/1998 |
| | 2002/0142569 A1 | 10/03/2002 | Chang | 03/29/2001 |
| | 2002/0146885 A1 | 10/10/2002 | Chen | 04/03/2002 |
| | 2002/0151138 A1 | 10/17/2002 | Liu | 04/10/2002 |
| | 2002/0168875 A1 | 11/14/2002 | Chang | 05/10/2001 |
| | 2002/0177275 A1 | 11/28/2002 | Liu | 05/28/2002 |
| | 2002/0182829 A1 | 12/05/2002 | Chen | 05/31/2001 |
| | 2003/0040152 A1 | 02/27/2003 | Liu | 08/22/2001 |
| | 2003/0057997 A1 | 03/27/2003 | Sun | 10/18/2002 |
| | 2003/0067807 A1 | 04/10/2003 | Lin | 10/22/2001 |
| | 2003/0117861 A1 | 06/26/2003 | Maayan | 12/20/2001 |
| | 4,184,207 | 01/15/1980 | McElroy | 07/12/1978 |
| | 4,420,504 | 12/13/1983 | Cooper | 05/17/1982 |
| | 4,755,864 | 07/05/1998 | Ariizumi | 09/14/1987 |
| | 4,881,114 | 11/14/1989 | Mohsen | 05/16/1986 |
| | 5,241,496 | 08/31/1993 | Lowrey | 08/19/1991 |
| | 5,330,930 | 07/19/1994 | Chi | 12/31/1992 |
| | 5,378,647 | 01/03/1995 | Hong | 10/25/1993 |
| | 5,379,253 | 01/03/1995 | Bergemont | 06/01/1992 |
| | 5,397,725 | 03/14/1995 | Wolstenholme | 10/28/1993 |
| | 5,467,305 | 11/14/1995 | Bertin | 03/12/1992 |
| | 5,576,236 | 11/19/1996 | Chang | 06/28/1995 |
| | 5,768,192 | 06/16/1998 | Eitan | 07/23/1996 |
| | 5,792,697 | 08/11/1998 | Wen | 04/23/1997 |
| | 5,858,841 | 01/12/1999 | Hsu | 11/25/1997 |
| | 5,911,106 | 06/08/1999 | Tasaka | 08/29/1997 |
| | 5,946,558 | 08/31/1999 | Hsu | 05/30/1997 |
| | 5,966,603 | 10/12/1999 | Eitan | 06/11/1997 |
| | 5,994,745 | 11/30/1999 | Hong | 04/24/1995 |
| | 6,011,725 | 01/04/2000 | Eitan | 02/04/1999 |
| | 6,028,342 | 02/22/2000 | Chang | 02/11/1998 |
| | 6,030,871 | 02/29/2000 | Eitan | 05/05/1998 |
| | 6,044,022 | 03/28/2000 | Nachumovsky | 02/26/1999 |
| | 6,081,456 | 06/27/2000 | Dadashev | 02/04/1999 |
| | 6,108,240 | 08/22/2000 | Lavi | 02/04/1999 |
| | 6,133,102 | 10/17/2000 | Wu | 06/19/1998 |
| | 6,134,156 | 10/17/2000 | Eitan | 02/02/1999 |

| | | |
|--------------------|--|-----------------|
| Examiner Signature | | Date Considered |
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**INFORMATION DISCLOSURE
STATEMENT
FORM PTO-1449**

| | | | |
|--------------|------------|-------------|------------|
| 6,147,904 | 11/14/2000 | Liron | 02/04/1999 |
| 6,157,570 | 12/05/2000 | Nachumovsky | 02/04/1999 |
| 6,172,396 B1 | 01/09/2001 | Chang | 04/23/1998 |
| 6,174,758 B1 | 01/16/2001 | Nachumovsky | 03/03/1999 |
| 6,175,523 B1 | 01/16/2001 | Yang | 10/25/1999 |
| 6,181,597 B1 | 01/30/2001 | Nachumovsky | 02/04/1999 |
| 6,184,089 B1 | 02/06/2001 | Chang | 01/27/1999 |
| 6,201,282 B1 | 03/13/2001 | Eitan | 12/23/1999 |
| 6,201,737 B1 | 03/13/2001 | Hollmer | 04/26/2000 |
| 6,204,529 B1 | 03/20/2001 | Lung | 08/27/1999 |
| 6,207,504 B1 | 03/27/2001 | Hsieh | 12/30/1998 |
| 6,208,557 B1 | 03/27/2001 | Bergemont | 05/21/1999 |
| 6,215,702 B1 | 04/10/2001 | Derhacobian | 02/16/2000 |
| 6,218,695 B1 | 04/17/2001 | Nachumovsky | 06/28/1999 |
| 6,222,768 B1 | 04/24/2001 | Hollmer | 04/26/2000 |
| 6,240,020 B1 | 05/29/2001 | Yang | 10/25/1999 |
| 6,243,300 B1 | 06/05/2001 | Sunkavalli | 02/16/2000 |
| 6,251,731 B1 | 06/26/2001 | Wu | 07/13/1999 |
| 6,255,166 B1 | 07/03/2001 | Ogura | 12/28/1999 |
| 6,256,231 B1 | 07/03/2001 | Lavi | 02/04/1999 |
| 6,266,281 B1 | 07/24/2001 | Derhacobian | 02/16/2000 |
| 6,269,023 B1 | 07/31/2001 | Derhacobian | 10/23/2000 |
| 6,272,043 B1 | 08/07/2001 | Hollmer | 06/23/2000 |
| 6,275,414 B1 | 08/14/2001 | Randolph | 11/22/2000 |
| 6,282,118 B1 | 08/28/2001 | Lung | 10/06/2000 |
| 6,291,854 B1 | 09/18/2001 | Peng | 12/30/1999 |
| 6,297,096 B1 | 10/02/2001 | Boaz | 07/30/1999 |
| 6,303,436 B1 | 10/16/2001 | Sung | 09/21/1999 |
| 6,327,174 B1 | 12/04/2001 | Jung | 02/24/2000 |
| 6,348,711 B1 | 02/19/2002 | Eitan | 10/06/1999 |
| 6,392,930 B2 | 05/21/2002 | Jung | 01/09/2001 |
| 6,417,053 B1 | 07/09/2002 | Kuo | 11/20/2001 |
| 6,421,275 B1 | 07/16/2002 | Chen | 01/22/2002 |
| 6,429,063 B1 | 08/06/2002 | Eitan | 03/06/2000 |
| 6,432,778 B1 | 08/13/2002 | Lai | 08/07/2001 |
| 6,461,949 B1 | 10/08/2002 | Chang | 03/29/2001 |
| 6,468,864 B1 | 10/22/2002 | Sung | 08/10/2001 |
| 6,469,342 B1 | 10/22/2002 | Kuo | 11/20/2001 |
| 6,477,084 B2 | 11/05/2002 | Eitan | 02/07/2001 |
| 6,486,028 B1 | 11/26/2002 | Chang | 11/20/2001 |
| 6,487,050 B1 | 11/26/2002 | Liu | 12/28/1999 |
| 6,498,377 B1 | 12/24/2002 | Lin | 03/21/2002 |

| | | |
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| | | | | |
|--|--------------|------------|-------|------------|
| | 6,514,831 B1 | 02/04/2003 | Liu | 11/14/2001 |
| | 6,531,887 B2 | 03/11/2003 | Sun | 06/01/2001 |
| | 6,545,309 B1 | 04/08/2003 | Kuo | 03/22/2002 |
| | 6,548,425 B2 | 04/15/2003 | Chang | 05/10/2001 |
| | 6,552,287 B1 | 04/22/2003 | Eitan | 12/14/1998 |
| | 6,559,013 B1 | 05/06/2003 | Pan | 07/10/2002 |
| | 6,576,511 B2 | 06/10/2003 | Pan | 05/02/2001 |
| | 6,580,135 B2 | 06/17/2003 | Chen | 03/22/2002 |
| | 6,580,630 B1 | 06/17/2003 | Liu | 06/07/2002 |
| | 6,602,805 B2 | 08/05/2003 | Chang | 12/14/2000 |
| | 6,607,957 B1 | 08/19/2003 | Fan | 07/31/2002 |
| | 6,610,586 B1 | 08/26/2003 | Liu | 09/04/2002 |
| | 6,613,632 B2 | 09/02/2003 | Liu | 05/28/2002 |
| | 6,617,204 B2 | 09/09/2003 | Sung | 08/13/2001 |

| Foreign Patent References | | | | |
|----------------------------------|----------------|------------|-----------------------------|------------------|
| Examiner Initials | Foreign Patent | | Name | Publication Date |
| | Country | No. | | |
| | EP | 84303740.9 | American Microsystems, Inc. | 01/25/1985 |
| | EP | 90115805.5 | Kabushiki Kaisha Toshiba | 02/20/1991 |
| | EP | 01113179.4 | Infineon Technologies AG | 12/04/2002 |

| Other References | |
|-------------------------|---|
| Examiner Initials | Author, Title, Date, Pages, etc. |
| | B. Eitan et al., "Characterization of Channel Hot Electron Injection by the Subthreshold Slope of NROM™ Device," IEEE Electron Device Lett., Vol. 22, No. 11, (Nov. 2001) pp. 556-558, Copyright 2001 IEEE. |
| | B. Eitan et al., "Spatial Characterization of Hot Carriers Injected into the Gate Dielectric Stack of a MOFSET Based on Non-Volatile Memory Device," date unknown, pp. 58-60. |
| | B. Eitan et al., "NROM: A Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell," IEEE Electron Device Lett., Vol. 21, No. 11, (Nov. 2000), pp. 543-545, Copyright 2000 IEEE. |
| | E. Maayan et al., "A 512Mb NROM Flash Data Storage Memory with 8MB/s Data Range," Dig. IEEE Int. Solid-State Circuits Conf., San Francisco, (Feb 2002), pp. 1-8, Copyright Saifun Semiconductors Ltd. 2002. |
| | E. Maayan et al., "A 512Mb NROM Flash Data Storage Memory with 8MB/s Data Range," ISSCC 2002 Visuals Supplement, Session 6, SRAM and Non-Volatile Memories, 6.1 and 6.2, pp. 76-77, 407-408. Copyright 1990 IEEE. |

| | | |
|---|--|-----------------|
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| | |
|--|--|
| | M. Janai, "Data Retention, Endurance and Acceleration Factors of NROM Devices," IEEE 41 st Annual International Reliability Physics Symposium, Dallas, TX (2003), pp. 502-505, Copyright 1989 IEEE. |
| | S. Minami and Y. Kamigaki, "A Novel MONOS Nonvolatile Memory Device Ensuring 10-Year Data Retention after 10 ⁷ Erase/Write Cycles," IEEE Transactions on Electron Devices, Vol. 40, No. 11 (Nov. 1993) pp. 2011–2017, Copyright 1998 IEEE. |
| | C. Pan, K. Wu, P. Freiberger, A. Chatterjee, G. Sery, "A Scaling Methodology for Oxide-Nitride-Oxide Interpoly Dielectric for EPROM Applications," IEEE Transactions on Electron Devices, Vol. 37, No. 6, (June 1990), pp. 1439-1443, Copyright 1990 IEEE. |
| | P. Manos and C. Hart, "A Self-Aligned EPROM Structure with Superior Data Retention," IEEE Electron Device Letters, Vol. 11, No. 7, (July 1990) pp. 309-311, Copyright 1990 IEEE |
| | W. Owen and W. Tchon, "E ² PROM Product Issues and Technology Trends," IEEE 1989, pp. 17-19, Copyright 1989 IEEE. |
| | T. Huang, F. Jong, T. Chao, H. Lin, L. Leu, K. Young, C. Lin, K. Chiu, "Improving Radiation Hardness of EEPROM/Flash Cell BY N ₂ O Annealing," IEEE Electron Device Letters, Vol. 19, No. 7 (July 1998), pp. 256-258, Copyright 1998 IEEE. |
| | B. Eitan et al., "Electrons Retention Model for Localized Charge in Oxide –Nitride-Oxide (ONO) Dielectric," IEEE Device Lett., Vol. 23, No. 9, (Sept. 2002), pp.556-558. Copyright 2002 IEEE. |
| | T. Nozaki, T. Tanaka, Y. Kijija, E. Kinoshita, T. Tsuchiya, Y. Hayashi, "A 1-Mb EEPROM with MONOS Memory Cell for Semiconductor Disk Application," IEEE Journal of Solid-State Circuits, Vol. 26, No. 4 (April 1991), pp. 497-501, Copyright 1991 IEEE. |
| | F. Vollebregt, R. Cuppens, F. Druyts, G. Lemmen, F. Verberne, J. Solo, "A New E(E)PROM Technology With A TiSi ₂ Control Gate," IEEE 1989, pp. 25.8.1 – 25.8.4, Copyright 1989 IEEE. |
| | B. Eitan et al., "Impact of Programming Charge Distribution on Threshold Voltage and Subthreshold Slope of NROM Memory cells," IEEE Transactions on Electron Devices, Vol. 49, No. 11, (Nov. 2002), pp. 1939-1946, Copyright 2002 IEEE. |
| | B. Eitan et al., "Spatial characterization of Channel hot electron injection utilizing subthreshold slope of the localized charge storage NROM™ memory device," Non-Volatile Semiconductor Memory Workshop (NVSMW), Monterey, CA, (Aug. 2001), pp. 1-2. |
| | B. Eitan et al., "Can NROM, a 2-bit, Trapping Storage NVM Cell, Give a Real Challenge to Floating Gate Cells?" Int. Conf. on Solid State Devices and Materials, Tokyo, (1999), pp. 1-3, Copyright 1999 Saifun Semiconductors Ltd. |
| | S. Ogura, et al. "Twin MONOS Cell with Dual Control Gates," Halo LSI and New Halo, pp 187 –187.3, Date Unknown. |
| | T. Sugizaki, et al. "New 2-bit/Tr MONOS Type Flash Memory using Al ₂ O ₃ as Charge Trapping Layer," Fujitsu Laboratories Ltd, Date Unknown. |
| | T. Saito, et al. "Hot Hole Erase Characteristics and Reliability in Twin MONOS Device" Halo LSI, Date Unknown. |

| | | |
|--------------------|--|-----------------|
| Examiner Signature | | Date Considered |
|--------------------|--|-----------------|

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| | |
|--|---|
| | Saifun Semiconductors, LTD. PowerPoint Presentation, Date Unknown |
| | Y. Roizin, et al. "Novel Techniques for data retention and Leff measurements in two bit <i>MicroFlash®</i> Memory Cells," Characterization and Metrology for ULSI Technology: 200 International Conf., pp. 181-185, Copyright 2001 American Institute of Physics, 1-56396-967-X/01. |
| | W. J. Tsai, et al. "Cause of Data Retention Loss in a Nitride-Based Localized Trapping Storage Flash Memory Cell," IEEE 40 th Annual International Reliability Physics Symposium, Dallas, (2002), pp. 34-38. Copyright 2002 IEEE. |
| | W.J. Tsai, et al. "Data Retention Behavior of a SONOS Type Two-Bit Storage Flash Memory Cell," IEDM 01-0179-01-722, Copyright 2001 IEEE. |
| | A. Shappir, et al., "Subthreshold slope degradation model for localized-charge-trapping based non-volatile memory devices," Solid-State Electronics 47 (2003), pp. 937-941. Copyright 2003 Elsevier Science Ltd. |
| | R. Neale, "AMD's MirrorBit – a big step in Flash progress," Electronic Engineering Design, V. 74, No. 906, pp. 47-50. |
| | I. Bloom, et al., "NROM™ -a new technology for non-volatile memory products" Solid-State Electronics 46 (2002), pp. 1757-1763. Copyright 2002 Elsevier Science Ltd. |
| | J. Bu and M. White, "Electrical characterization on ONO triple dielectric in SONOS nonvolatile memory devices," Solid-State Electronics 45 (2001) pp. 47-51. Copyright 2001 Elsevier Science Ltd. |
| | Y. Kamigaki and S. Minami, "MNOS Nonvolatile Semiconductor Memory Technology: Present and Future," IEICE Trans. Electron, Vol. E84-C, No. 6, pp. 713-723 (June 2001) |
| | E. Lusky, et al., "Electron Discharge Model of Locally-Trapped Charge in Oxide-Nitride-Oxide (ONO) Gates for NROM™ Non-Volatile Semiconductor Memory Devices," Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, Tokyo, 2001 pp. 534-535. |
| | A. Nughin, "n-Channel 256kb and 1Mb EEPROMs," ISSCC91, Session 134, Special Session on Technology in the USSR, Paper 13.4, 1991 IEEE InternationalSolid State Circuits Conference, Digest of Technical Papers, pp. 228-229, 319 |
| | G. Xue, et al., "Low Voltage Low Cost Nitride Embedded Flash Memory Cell" IMEC., Date Unknown. |
| | L. Breuil, et al., "A new 2 isolated-bits/cell flash memory device with self aligned split gate structure using ONO stacks for charge storage," IMEC, Date Unknown. |
| | J. Willer, et al., "UMEM: A U-shape Non-Volatile-Memory Cell," Ingentix GmbH &Co. KG., Infineon Technologies and Saifun Semiconductors, Date Unknown |
| | S. Kang, et al., "A Study of SONOS Nonvolatile Memory Cell Controlled Structurally by Localizing Charge-Trapping Layer," Samsung Electrons Co., Ltd., Date Unknown. |
| | Y. Roizin, et al., "In-Process Charging in <i>microFLASH®</i> Memory Cells," Tower Semiconductor, Ltd., Date Unknown |

| | | |
|--------------------|--|-----------------|
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| | |
|--|--|
| | A. Shappir, et al., "Subthreshold slope degradation model for localized-charge-trapping based non-volatile memory devices," Solid State Electronics, 47 (2003) pp. 937-941, Copyright 2003 Elsevier Science Ltd. |
| | I. Fujiwara, et al., "High speed program/erase sub 100 nm MONOS memory cell," Sony Corporation, Date Unknown |
| | E. Lusky, et al., "Investigation of Spatial Distribution of CHE Injection Utilizing the Subthreshold Slope and the Gate Induced Drain Leakage (GIDL) Characteristics of the NROM™ Device," Saifun Semiconductors, Ltd. and Tel Aviv University, Dept of Physical Electronics, pp. 1-2., Date Unknown |
| | C. C. Yeh, et al., "A Modified Read Scheme to Improve Read Disturb and Second Bit Effect in a Scaled MXVAND Flash Memory Cell," Macronix International Co., Ltd. and Department of Electronics Engineering, National Chiao-Tung University, Date Unknown. |
| | Y. K. Lee, et al., "30-nm Twin Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) Memory (TSM) with High Erase Speed and Reliability," School of Electrical Engineering, Seoul National University, C&M, System LSI, ATD, PD, Samsung Electronics Co., Date Unknown |
| | J. H. Kim, et al., "Highly Manufacturable SONOS Non-Volatile Memory for the Embedded SoC Solution," 2003 Symposium on VLSI Technology Digest of Technical Papers, pp. 31-32. |
| | Y. Hayashi, et al., "Twin MONOS Cell with Dual Control Gates," 2000 Symposium on VLSI Technology Digest of Technical Papers, 2000 IEEE, pp. 122-123. |
| | M. K. Cho and D. M. Kim, "High Performance SONOS Memory Cells Free of Drain Turn-On and Over-Erase: Compatibility Issue with Current Flash Technology," IEEE Electron Device Letters, Vol. 21, No. 8, August 2000, pp. 399-401, Copyright 2000 IEEE |
| | T. Y. Chan, K.K. Young and C. Hu, "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device," IEEE Electron Device Letters, Vol. EDL-8, No. 3, March 1987, pp. 93-95., Copyright 1987 IEEE. |
| | I. Bloom, et al., "NROM™ NVM technology for Multi-Media Applications," Saifun Semiconductors, Ltd. Ingentix, Ltd. and Infineon Technologies, Date Unknown |
| | E. J. Prinz, et al., "An Embedded 90nm SONOS Flash EEPROM Utilizing Hot Electron Injection Programming and 2-Sided Hot Hole Injection Erase," Motorola Embedded Memory Center, Date Unknown |
| | Y. Roizin, et al., "Retention Characteristics of <i>microFLASH®</i> Memory (Activation Energy of Traps in the ONO Stack)," Tower Semiconductor, Ltd., Date Unknown |
| | Y. Roizin, et al., "Activation Energy of Traps in the ONO Stack of <i>microFLASH®</i> Memory Cells," Tower Semiconductor, Ltd., Date Unknown |
| | Y. Roizin, et al., "'Dummy' Gox for Optimization of <i>microFLASH®</i> Technology," Tower Semiconductor, Ltd., Date Unknown |
| | Y. K. Lee, et al., "Multi-Level Vertical Channel SONOS Nonvolatile Memory on SOI," 2002 Symposium on VLSI Technology Digest of Technical Papers, Copyright 2002 IEEE. |
| | T. Saito, et al., "CHE Program Behavior in MONOS Device," Halo LSI., Date Unknown |

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|--|---|
| | J. Bu, et al., "Retention Reliability Enhanced SONOS NVSM with Scaled Programming Voltage," Microelectronics Lab., Date Unknown |
| | H. Tomiye, et al., "A novel 2-bit/cell MONOS memory device with a wrapped-control-gate structure that applies source-side hot-electron injection," 2002 Symposium on VLSI Technology Digest of Technical Papers, Copyright 2002 IEEE. |
| | Certified Translation, "Flash cell that seeks to replace current technology introduced enabling both low cost and high performance" Nikkei Microdevices, November 1999, pp. 147-148. |

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